Amendments to the Claims

1. (Currently Amended) A method for detecting signal strengths in a hardware description language ~~that does not provide for such detection~~, comprising:

creating a wired net configuration that provides for a data input signal and a controlled reference signal, wherein the controlled reference signal has a logical value opposite that of the input signal;

varying the controlled reference signal based on a desired signal strength to be detected, wherein the desired signal strength comprises a range of signal strengths, and wherein the controlled reference signal has a signal strength larger than the range of signal strengths; and

comparing the input signal with the controlled reference signal to determine if the desired signal strength has been detected.

2. (Original) The method of claim 1, wherein the hardware description language comprises Verilog.

3. (Cancelled).

4. (Cancelled).

5. (Currently Amended) ~~The method of claim 1,~~ A method for detecting signal strengths in a hardware description language, comprising:

creating a wired net configuration that provides for a data input signal and a controlled reference signal;

varying the controlled reference signal based on a desired signal strength to be detected; and

comparing the input signal with the controlled reference signal to determine if the desired signal strength has been detected;

wherein the controlled reference signal has a logical value opposite that of the input signal, and wherein the controlled reference signal has a signal strength exactly opposite the desired signal strength to be detected.

6. (Original) The method of claim 1, wherein the comparing further comprises:

inputting the input signal and the controlled reference signal into a first wired net;

resolving the first wired net to obtain a resolved value;

inputting a signal corresponding to the input signal into a scalar net; and

comparing the resolved value on the first wired net with the signal corresponding to the input signal on the scalar net to determine if the desired signal strength has been detected.

7. (Currently Amended) A module for detecting signal strengths in a hardware description language ~~that does not provide for such detection~~, the module comprising:

a first wired net for receiving an input signal and a controlled reference signal, wherein the hardware description language resolves the first wired net to obtain a resolved value, and wherein the controlled reference signal has a logical value opposite that of the input signal;

a scalar net for receiving a signal corresponding to the input signal; and

a comparison system for comparing the resolved value on the first wired net with the signal corresponding to the input signal on the scalar net to determine if a desired signal strength has been detected, wherein the desired signal strength comprises a range of signal strengths, and wherein the controlled reference signal has a signal strength larger than the range of signal strengths.

8. (Original) The module of claim 7, wherein the hardware description language comprises Verilog.

9. (Cancelled).

10. (Cancelled).

11. (Currently Amended) ~~The module of claim 7~~ A module for detecting signal strengths in a hardware description language, the module comprising:

a first wired net for receiving an input signal and a controlled reference signal, wherein the hardware description language resolves the first wired net to obtain a resolved value, and wherein the controlled reference signal has a logical value opposite that of the input signal;

a scalar net for receiving a signal corresponding to the input signal; and

a comparison system for comparing the resolved value on the first wired net with the signal corresponding to the input signal on the scalar net to determine if a desired signal strength has been detected, ~~and~~ wherein the controlled reference signal has a signal strength exactly opposite the desired signal strength to be detected.

12. (Original) The module of claim 7, wherein the input signal is input into the first wired net via an isolating element.

13. (Original) The module of claim 7, wherein the controlled reference signal is provided via a buffer, wherein the input of the buffer is tied to one of a source voltage and ground.

14. (Original) The module of claim 7, wherein the signal corresponding to the input signal is produced by inputting the input signal into a buffer.

15. (Original) The module of claim 7, wherein the comparison system comprises a vector comparison block for comparing a vector composed of the resolved value on the first wired net and the signal corresponding to the input signal on the scalar net to a predetermined key combination.

16. (Original) The module of claim 7, wherein the desired signal strength is selected from the group consisting of: supply0, strong0, pull0, large0, weak0, medium0, small0, supply1, strong1, pull1, large1, weak1, medium1, and small1.

17. (Currently Amended) A program product stored on a recordable medium for detecting signal strengths, comprising:

program code for providing a first wired net for receiving an input signal and a controlled reference signal and for resolving the first wired net to obtain a resolved value, wherein the controlled reference signal has a logical value opposite that of the input signal;

program code for providing a scalar net for receiving a signal corresponding to the input signal; and

program code for comparing the resolved value on the first wired net with the signal corresponding to the input signal on the scalar net to determine if a

desired signal strength has been detected, wherein the desired signal strength comprises a range of signal strengths, and wherein the controlled reference signal has a signal strength larger than the range of signal strengths.

18. (Original) The program product of claim 17, wherein the hardware description language comprises Verilog.

19. (Cancelled).

20. (Cancelled).

21. (Currently Amended) ~~The program product of claim 17~~ A program product stored on a recordable medium for detecting signal strengths, comprising:

program code for providing a first wired net for receiving an input signal and a controlled reference signal and for resolving the first wired net to obtain a resolved value;

program code for providing a scalar net for receiving a signal corresponding to the input signal; and

program code for comparing the resolved value on the first wired net with the signal corresponding to the input signal on the scalar net to determine if a desired signal strength has been detected, wherein the controlled reference signal has a logical value opposite that of the input signal, and wherein the

controlled reference signal has a signal strength exactly opposite the desired signal strength to be detected.

22. (Original) The program product of claim 17, wherein the program code for comparing further comprises program code for comparing a vector composed of the resolved value on the first wired net and the signal corresponding to the input signal on the scalar net to a predetermined key combination.

23. (Currently Amended) ~~A reusable module for detecting signal strengths in Verilog, the reusable module comprising:~~

~~a first wired net for receiving an input signal and a controlled reference signal, wherein the hardware description language resolves the first wired net to obtain a resolved value;~~

~~a scalar net for receiving a signal corresponding to the input signal; and~~

~~a comparison system for comparing the resolved value on the first wired net with the signal corresponding to the input signal on the scalar net to determine if a desired signal strength has been detected~~ The module of claim 7, wherein the module is reusable, and wherein the desired signal strength is selected from the group consisting of: supply0, strong0, pull0, large0, weak0, medium0, small0, supply1, strong1, pull1, large1, weak1, medium1, small1, and ranges of signal strengths.